Embedded based Signal Filtration using LabVIEW

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Abstract: This paper represents the filtration process of a sinusoidal signal using Direct Digital Synthesizer (DDS) and Finite Impulse Response (FIR) Compiler. The system functions on both hardware as well as software. The hardware includes NI PXIe-1075 and the software as LabVIEW. The hardware consists of various chassis which involves controlling, amplifying, up-converting, down-converting and a baseband transceiver system. The software used is LabVIEW software in both FPGA and RT environment. Both hardware and software are being interfaced through an Ethernet cable for the medium of data transfer. The process involves generation of a target and a host in LabVIEW software for signal filtration and later dumping into the hardware to observe the filtered output. The whole system is performed in order to eliminate unwanted signal from that of the original ones. It can be very much effective for the reliable mode of communication in a wireless channel.

Key words- FIR compiler, FPGA, LabVIEW

Introduction

Embedded system itself means a combined system of both hardware and software. In this paper there is a systematic procedure for filtration of a signal by using LabVIEW software and FPGA hardware as NI PXIe1075. Signal filtration is very essential for removing any kind of unwanted signal combined with the necessary information. There are various methods for filtration process using Low pass filter, high pass filter, band pass filter, band stop filter, Butterworth filter, FIR filter, IIR filter and many more. Here we perform a simulation for filtering a sinusoidal signal using FIR filter. FIR stands for Finite Impulse Response. It provides finite impulse responses which do not have a feedback. FIR is generally used for any kind of filter realization. But the main disadvantage is that it takes more computational power for the processor to run. In LabVIEW filtration is carried out by FIR compiler. FIR compiler provides high performance finite impulse response and a user interface to generate highly parameterizable filter. This compiler can support serial as well as parallel implementation. It involves generation of analog signal by DDS compiler. The NI hardware consists of various FPGA modules which perform controlling of the embedded system, RS 485/RS 422 and RS 232 Connector, RF Pre-amplifier, RF Down converter, Baseband Transceiver and RF Up converter.

Methodology

The main purpose is to generate a sinusoidal signal and filtering the same with the FIR filter using FIR Compiler. The working principle behind the whole system involves creating VIs in FPGA and RT environment. Here the user develops VI for creating FPGA target and the RT host which in turn dumped into the hardware for total simulation. The process began with the creating a new project in LabVIEW and developing a VI as shown in Fig. 1, Fig. 2, Fig. 3.

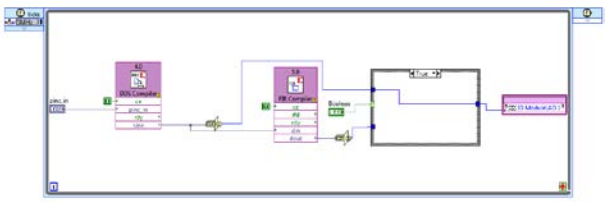

Fig. 1 Creating VI in FPGA target (when FALSE)

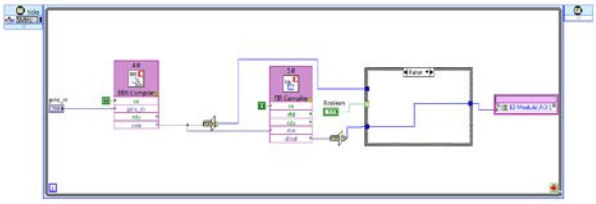

Fig. 2 VI FPGA target (when TRUE)

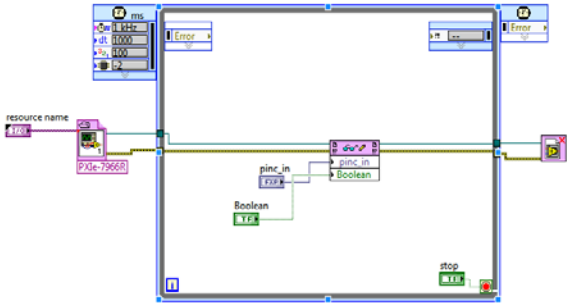

Fig. 3 Generating a RT Host for target

A single cycle timed loop running at 5MHz clock frequency. The DDS compiler was opened and configured accordingly by selecting sinusoidal signal for waveform generation. The coefficient was exported from the LabVIEW examples and the filter was configured by selecting filter type as band pass, giving input in pass band edge frequency (20 kHz, 30 kHz) and stop band edge frequency (15 kHz, 35 kHz)and sample frequency to 100 kHz. The VI was run and the generated coefficient was saved at a particular location. Then the FIR compiler was opened and configured by providing input sampling frequency as 100 kHz and the location of filter coeffient. An I/O module was connected to observe the output at oscilloscope. And the further connections were made as per Fig. 1. Fig. 2 indicates when the case function is in true state. The VI was run and the bit file was saved. Fig. 3 indicates the RT host for the target. Here we add a FPGA Reference VI where we dumped the bit file as saved before and a read write control and a constant of resource name was connected as shown then VI was finally run to observe the output.

Result

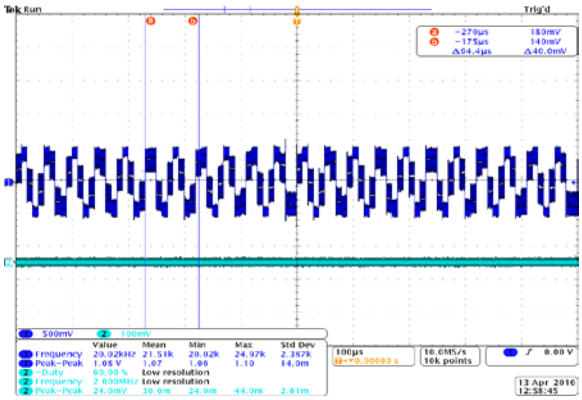

Fig. 4 Sinusoidal signal of 22 kHz with distortion when filter was OFF

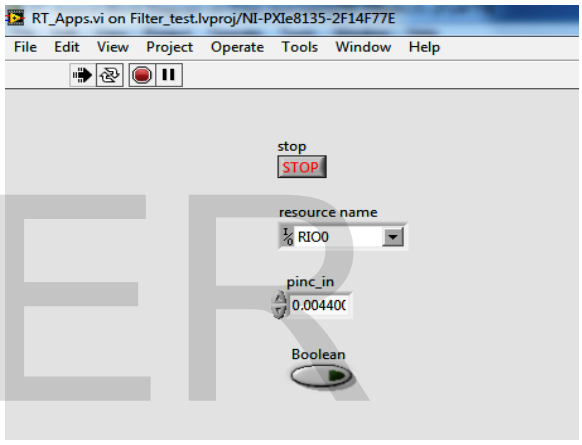

Fig. 5 Front panel when filter is OFF

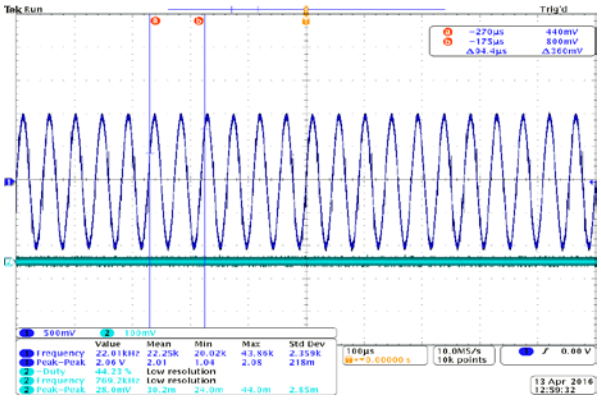

Fig. 6 FIR filtered sinusoidal signal when filter was ON

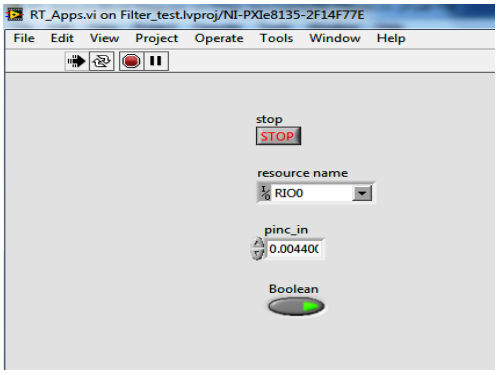

Fig. 7 Front panel when filter is ON

Fig. 4 indicates a generated sinusoidal signal of 22 kHz with noise on the oscilloscope. Fig. 5 indicates the front panel of the LabVIEW when filter is OFF. Fig. 6 shows the filtered sinusoidal signal when the filter is ON. Fig. 7 indicates the front panel view when the filter is ON.

Discussion

From the above methodology it clearly states that by the means of filtration technique we can filter any kind of unwanted signal which is combined with our message signal. By the effective use of the FIR compiler we can vary sample frequency and the filter type according to the user's choice. The compilation time depends upon the processor used in the system. Otherwise it is easier and faster to implement any kind of filter which is necessarily required. So filtration technique could be the best way for reception of noiseless signal which could be very effective for a reliable communication. This application can be implemented for future use in telecommunication, military and navigation field so that we receive original information at the receiver end.

Conclusion

In today's era FPGA plays an important role in providing a basic platform for high performance evaluation in an optimized area. FPGA are very flexible and provides rapid prototyping with less power consumption. The main motive of this paper states that we need to filter out various unwanted and distorted signal at the receiver side. So we need to design such kind of filter which can effectively work in various communication fields only by varying some parameters to filter the unwanted signal according to the user's requirement.

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About the Author

Pranita Behera received her B. Tech degree in Electronics and Telecommunication Engineering at Trident Academy of Technology, Bhubaneswar under Biju Patnaik University of Technology, Rourkela in 2013-14. She is currently pursuing her Master's degree in Electronics and Communication Engineering at Sikkim Manipal Institute of Technology, Majhitar, Sikkim. Her work experience and training is based on the telecommunication at BSNL, Bhubaneswar, Odisha and time dissimination system through RF signal at DRDO, Chandipur, Balasore, Odisha.